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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GOOD JOHNSON, MOTILEWA	

ART UNIT	PAPER NUMBER
2677	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,860	SUN, WEIN-TOWN	
	Examiner	Art Unit	
	Motilewa Good-Johnson	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8,9,12,13 and 15-17* is/are rejected.

7)☒ Claim(s) *5,7,10,11,14 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6, 8, 9, 12, 13 and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Maruoka et al., U.S. Patent Publication Number 2002/0186192 A1.

Regarding claim 1, Maruoka discloses a power-saving circuit for an active matrix liquid crystal display ("LCD") panel (figure 1, element 100), comprising: a plurality of first capacitors (figure 34, element 53), each first capacitor corresponding to a data line of the LCD panel for collecting electrical charge provided on an associated data line (figure 33); at least one set of second capacitors (figure 34, element 54); at least one set of transistors (figure 33, element 30), each transistor of a set corresponding to one of the plurality of first capacitors (figure 33); and at least two control signals, each control signal corresponding to a set of the at least one set of transistors and corresponding to a set of the at least one set of second capacitors, and each control signal functioning to switch between a first and a second state to control the operation state of an associated set of transistors (paragraph 0156), wherein the at least two control signals switch to a

first state in a first sequence starting from a first control signal to a last control signal, and then in a second sequence starting from the last control signal to the first control signal, the first sequence alternating with the second sequence (paragraphs 0146, 0158)

Regarding claim 2, Maruoka discloses wherein each second capacitor of a set in response to a first state of an associated control signal reaches a voltage level that is an average of a voltage level of the each second capacitor held at a previous first state of the associated first control signal and a voltage level of an associated first capacitor in proportion to the capacitance values of the each second capacitor and the associated first capacitor (paragraphs 0149-0152)

Regarding claim 3, Maruoka discloses wherein each transistor includes a gate coupled to an associated control signal, a first terminal coupled to an associated first capacitor, and a second terminal coupled to an associated second capacitor (paragraph 0169)

Regarding claim 4, Maruoka discloses wherein the second terminals of a subset of transistors of a set are coupled to a same second capacitor (figure 34A)

Regarding claim 6, Maruoka discloses wherein the first and second capacitance values are predetermined (paragraph 0190)

Regarding claim 8, Maruoka discloses wherein a set of second capacitors is formed between a data driver and a cell matrix driven by the data driver of the LCD panel (figure 33, paragraph 0144)

Regarding claim 9, Maruoka discloses a power-saving circuit for an active matrix liquid crystal display ("LCD") panel (figure 1, element 100), comprising: a plurality of first capacitors (53), each first capacitor corresponding to a data line of the LCD panel for collecting electrical charge provided on an associated data line (paragraph 0146); a plurality of second capacitors (54); a plurality of transistors, each transistor including a gate, a first terminal coupled to one of the plurality of first capacitors, and a second terminal coupled to one of the plurality of second capacitors (paragraph 0156); and a control signal coupled to the gates of the plurality of transistors, and functioning to switch between a first and a second state to control the operation state of the plurality of transistors (paragraph 0146), wherein each second capacitor in response to a first state of the control signal reaches a voltage level that is an average of a voltage level of the each second capacitor held at a previous first state of the control signal and a voltage level of an associated first capacitor in proportion to the capacitance values of the each second capacitor and the associated first capacitor (paragraph 0158)

Regarding claim 12, Maruoka discloses wherein the second terminals of a subset of the plurality of transistors are coupled to a same second capacitor (paragraph 0146)

Regarding claim 13, Maruoka discloses wherein the number of the plurality of transistors is same as that of the plurality of second capacitors (figure 33)

Regarding claim 15, Maruoka discloses a method of power saving for an active matrix liquid crystal display ("LCD") panel (figure 1, element 100) comprising; providing a plurality of first capacitors (figure 34, element 53); electrically coupling each first capacitor to a data line of the LCD panel (figure 33); providing at least one set of transistors (figure 33, element 30); electrically coupling each transistor of a set to one of the plurality of first capacitors (figure 34A); providing at least one set of second capacitors (figure 34A); electrically coupling each set of second capacitors to a set of transistors (figure 34A); providing at least one control signal; electrically coupling each control signal to a set of transistors (paragraph 0156), each control signal functioning to switch between a first and a second state to control the operation state of an associated set of transistors; switching the at least one control signal to a first state in a first sequence starting from a first control signal to a last control signal such that voltage levels of a second capacitor and an associated first capacitor are averaged in proportion to their respective capacitance values; and switching the at least one control signal in a second sequence starting from the last control signal to the first control signal such that voltage levels of a second capacitor and an associated first capacitor are averaged in proportion to their respective capacitance values (paragraph 0146-0156)

Regarding claim 16, Maruoka discloses further comprising repeating the first and second sequences (paragraph 0146)

Regarding claim 17, Maruoka discloses further comprising coupling a gate of each transistor of a set to an associated control signal coupling a first terminal of the each transistor of a set to an associated first capacitor, and coupling a second terminal of the each transistor of a set to an associated second capacitor (paragraphs 0144 and 0148)

Allowable Subject Matter

3. Claims 5, 7, 10, 11, 14 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter:

The prior art cited fails to render obvious the first and second capacitor value as substantially the same, the claimed first and second control swings of the voltage level the first controls signals and at least two transistors set to a same capacitor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Motilewa Good-Johnson whose telephone number is (571) 272-7658. The examiner can normally be reached on Monday, Tuesday and Wednesday 9:00 AM - 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Motilewa Good-Johnson
Examiner
Art Unit 2677

mgj

AMR A. AWAD
PRIMARY EXAMINER